* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] Said processing process is the manufacture approach of the semiconductor device characterized by to form a mask layer or an etching stopper layer in the level difference section upper part of a processed layer in which the level difference section was beforehand formed in the manufacture approach of a semiconductor device including the processing process which performs processing of said level difference circles of the processed layer which has the level difference section, and to perform processing of said level difference circles using said mask layer or a stopper layer.
[Claim 2] The 1st process at which said processing process forms the flattening layer which carries out flattening of said level difference section on the processed layer in which the level difference section was formed beforehand, The 2nd process which carries out pattern NINGU of said flattening layer, The manufacture approach of the semiconductor device according to claim 1 characterized by being carried out by performing the 3rd process which performs processing of level difference circles of said processed layer by using as a mask layer or an etching stopper layer said flattening layer by which pattern NINGU was carried out.
[Claim 3] The flattening layer in said 1st process is the manufacture approach of the semiconductor device according to claim 2 characterized by applying, and drying and forming a liquefied constituent.
[Claim 4] Said liquefied constituent in said 1st process is the manufacture approach of the semiconductor device according to claim 3 characterized by being a thing containing a silicon compound.
[Claim 5] The manufacture approach of the semiconductor device according to claim 4 characterized by having the denaturation process which denatures said flattening layer by which pattern NINGU was carried out after said 2nd process and before the 3rd process.
[Claim 6] The manufacture approach of the semiconductor device according to claim 5 characterized by performing at least one of oxidation of said flattening layer, nitriding, and the carbonization in said denaturation process.
[Claim 7] Said silicon compound is the manufacture approach of the semiconductor device according to claim 4 characterized by being either an organic silicon oxide or an organic silicon compound.
[Claim 8] In the manufacture approach of a semiconductor device including the processing process which performs processing of level difference circles of the processed layer which has the level difference section said processing process The 1st process which applies and dries the liquefied constituent which contains a silicon compound in the processed layer in which the level difference section was formed beforehand, and forms a silicon compound layer, The 2nd process which carries out pattern NINGU of said silicon compound layer, oxidizes and makes said silicon compound layer by which pattern NINGU was carried out a silicon oxide layer, The manufacture approach of the semiconductor device characterized by having the 3rd process which performs processing of level difference circles of said processed layer by using said silicon oxide layer as an etching stopper layer or a mask layer.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention is concerned with the manufacture approach of a semiconductor device.
[0002]
[Description of the Prior Art] etching the film which formed membranes further or was formed of the membrane formation all over the slot, processing of level difference circles, for example, the hole, of the processed layer in which the level difference sections, such as holes, such as the time of deep formation of a trench mold capacitor, and a slot, were formed, **** -- etc. -- it may be necessary to process it The example is explained using drawing 3 and 4.
[0003] The sectional view showing one process of the conventional trench capacitor formation process in drawing 3 and drawing 4 is shown. for example, in drawing 3 , the trench 2 is formed in the silicon substrate 1, the SiN layer 3 is formed in the wall of a trench 2, and the part further boiled in the SiN layer 3 is filled up with N+ polish recon layer 4.
[0004] In drawing 4 , i-polish recon layer 5 is formed on N+ polish recon layer 4 in N+ polish recon layer 3 in the trench 2 formed in the silicon substrate 1 of drawing 3 .
[0005] Membrane formation and etching of i-polish recon layer 5 were performed to the level difference circles which consist of a trench 2 shown in drawing 3 , and it had passed through the process as shown in drawing 5 conventionally to form structure as shown in drawing 4 R> 4 with a sufficient precision.
[0006] first, the SiO two-layer which acts as a mask beforehand in the case of formation of etching of the SiN layer 6 and trench 2 which act as a mask layer at the etching process of next i-polish recon layer 5 on a silicon substrate 1 as shown in drawing 5 (1) -- the laminating of 7 is carried out, it is formed and pattern NINGU is carried out by the photolithography using a resist layer (not shown).
[0007] next, it is shown in drawing 5 (2) -- as -- SiO two-layer -- it etches by using 7 as a mask, and the deep trench 2 is formed.
[0008] By passing through further two or more processes, as shown in drawing 5 (3) (it is the same as that of drawing 3), the SiN layer 3 is formed in the wall of a trench 2, and the structure where it filled up with N+ polish recon layer 4 in the SiN layer 3 further is formed. Since SiO two-layer 7 has the intense damage in the case of etching of a trench 2, it exfoliates in fluoric acid processing, and it makes the SiN layer 6 remain on silicon substrate 1 front face.
[0009] Next, processing in a trench 2 is performed.
[0010] As shown in drawing 5 (4), i-polish recon layer 5 is formed on N+ polish recon layer 4 in a trench 2.
[0011] Next, as shown in drawing 5 (5), i-polish recon layer 5 front face is ground, the SiN layer 6 is exposed, and flattening is carried out.
[0012] Next, as shown in drawing 5 (6), it etches using the SiN layer 6 as a mask layer, and desired structure (it is the same as that of drawing 4) is acquired. Finally the SiN layer 6 exfoliates at a back process.
[0013] thus, the SiO two-layer used as the mask layer at the time of conventionally etching the trench 2 which is the process before forming the level difference section which consists of a trench 2 the SiN layer 6 which turns into a mask layer in case processing of etching in the trench 2 as shown in drawing 5 (6) etc. is needed, and is shown in drawing 5 (2) -- the laminating was carried out to 7 and it formed.
[0014] the SiO two-layer which is shown in drawing 5 (1) in on the other hand forming the deep trench 2 as detailed-ization of a semiconductor device progresses -- in case the mask layer of the two-layer structure which consists of 7 and a SiN layer 6 is formed, it is necessary to perform etching of the high aspect ratio in a thin resist layer however --

although a resist and SiO two-layer etch selectivity is comparatively high -- the etch selectivity of a resist and a SiN layer -- low -- SiO two-layer -- it is becoming difficult to carry out pattern NINGU of the mask layer of the two-layer structure which consists of 7 and a SiN layer 6, and to form the high pattern of an aspect ratio especially in the SiN layer 6.

[0015] The ** which does not use the SiN layer 6 as a mask layer in case processing in a trench 2 is performed, the SiO two-layer used as the mask layer at the time of etching a trench 2, although the above-mentioned trouble will not be produced if 7 is used as a mask layer in case processing in a trench 2 is performed as it is Since SiO two-layer 7 has the intense damage in the case of etching of a trench 2, if it is used as it is, it cannot carry out high processing of precision to processing in a trench 2. therefore, SiO two-layer -- 7 -- after termination of etching of a trench 2 -- exfoliating -- SiO two-layer -- the above-mentioned method of preparing beforehand as a mask layer of processing of the SiN layer 6 which is an ingredient which is different in 7 in a trench 2 must be taken.

[0016] thus, by the approach of establishing before level difference section formation, the mask layer or etching stopper layer used for processing of level difference circles For example, since damage on the mask layer for level difference section formation arises like the above, It does not obtain. the mask layer or etching stopper layer used for processing of level difference circles using the ingredient which is an ingredient different from the mask layer for level difference section formation -- beforehand -- not forming -- The high pattern of an aspect ratio cannot be formed in the mask layer or etching stopper layer used for processing of level difference circles in connection with it, Since the constraint on a process arises in the ingredient and thickness of the layer used as the mask layer used for processing of level difference circles, or an etching stopper layer, process tolerance -- the mask layer or etching stopper layer for processing of level difference circles could not be formed highly, but there was a trouble that it could not respond to detailed-ization of a semiconductor device.

[0017]

[Problem(s) to be Solved by the Invention] the ingredient of the mask used in case processing of the processed film which this invention was made in view of the above-mentioned trouble, and has the level difference section of said level difference circles is performed, or an etching stopper layer, and the width of face of selection of thickness -- extending -- process tolerance -- a mask or an etching stopper layer can be formed highly, and it is in offering the manufacture approach of the semiconductor device which can respond to detailed-ization of a semiconductor device.

[0018]

[Means for Solving the Problem] In the manufacture approach of a semiconductor device that this invention includes the processing process which performs processing of said level difference circles of the processed layer which has the level difference section, said processing process is the manufacture approach of the semiconductor device characterized by to form a mask layer or an etching stopper layer in the level difference section upper part of a processed layer in which the level difference section was formed beforehand, and to perform processing of said level difference circles using said mask layer or a stopper layer.

[0019] In the manufacture approach of a semiconductor device that this invention includes the processing process which performs processing of level difference circles of the processed layer which has the level difference section moreover, said processing process The 1st process which applies and dries the liquefied constituent which contains a silicon compound in the processed layer in which the level difference section was formed beforehand, and forms a silicon compound layer, The 2nd process which carries out pattern NINGU of said silicon compound layer, oxidizes and makes said silicon compound layer by which pattern NINGU was carried out a silicon oxide layer, It is the manufacture approach of the semiconductor device characterized by having the 3rd process which performs processing of level difference circles of said processed layer by using said silicon oxide layer as an etching stopper layer or a mask layer.

[0020] In processing membrane formation or etching into said level difference circles of the processed layer which has the level difference section, i.e., a hole, or a slot in this invention, formation of the mask layer for said processing or an etching stopper layer is performed after level difference section formation. thereby -- the ingredient of said mask layer or an etching stopper layer, and the width of face of selection of thickness -- it can extend -- process tolerance -- a mask layer or an etching stopper layer can be formed highly, and it can respond to detailed-ization of a semiconductor device.

[0021] By applying and drying the liquefied constituent containing a silicon compound, forming a silicon compound layer on said processed layer, oxidizing said silicon compound layer and forming said mask layer or an etching stopper

layer especially While a mask layer or an etching stopper layer excellent in etching resistance is obtained, said flat silicon compound layer with sufficient restoration nature can be formed in said level difference section, and in case it is pattern NINGU of said silicon compound layer, the operation as an acid-resisting layer of a resist layer is shown. Furthermore, the etch selectivity with an opposite resist of the silicon oxide layer in which said silicon compound layer comes to oxidize is also high. Therefore, a mask layer or an etching stopper layer can be formed in the processed layer which has the level difference section with sufficient process tolerance, and it can respond to detailed-ization of a semiconductor device.

[0022] In addition, especially this invention is effective in formation of a trench mold capacitor.

[0023]

[Embodiment of the Invention] This invention is used in case the processing process which includes etching in the level difference circles of a processed layer in which level difference section, for example, hole, or slot ** was formed beforehand is given. That is, in this invention, said processing process forms a mask layer or an etching stopper layer in the level difference section upper part of a processed layer in which the level difference section was formed beforehand as mentioned above, and performs processing of level difference circles using it.

[0024] In addition, in this invention, a processed layer can use the insulating layer which consists of an organic system ingredient or inorganic system ingredients, such as a conductive layer which consists of a wiring material formed on the silicon substrate and the silicon substrate, an electrode material, etc., polyimide, and SOG, or blank mask material.

[0025] As for the processing process of this invention, it is specifically desirable to perform the following 1st - the 3rd process.

[0026] (The 1st process) The 1st process forms in the level difference section upper part the flattening layer which covers and carries out flattening of said level difference section. In the 2nd process and the 3rd process which are mentioned later, pattern NINGU of said flattening layer is carried out, and it acts as a mask layer or an etching layer.

[0027] In the 1st process, it is desirable to apply and dry a liquefied constituent and to obtain said flattening layer on the processed layer in which said level difference section was formed desirably. Flattening of the level difference section can be carried out easily by that cause, and pattern NINGU for using a flattening layer as a mask or an etching stopper can be performed with a sufficient precision.

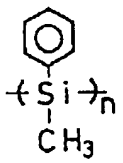
[0028] It is desirable to use what contains a silicon compound as said liquefied constituent. Thereby, said flattening layer turns into a silicon compound layer. In case exposure at the time of pattern NINGU for considering as a mask or an etching stopper by forming a silicon compound layer is performed, it can act as an antireflection film and pattern NINGU can be performed with a sufficient precision. Moreover, a mask or an etching stopper excellent in etching resistance can be formed.

[0029] As for said silicon compound, it is desirable that they are an organic silicon oxide or an organic silicon compound. The organic silicon oxide and the organic silicon compound are suitable for obtaining the liquefied constituent excellent in solubility. Said organic silicon compound is a compound with the direct coupling of carbon and silicon. Said organic silicon oxide is an oxide of an organic silicon compound. The high molecular compound which has Si-Si association in a principal chain with the direct coupling of carbon and silicon especially as said organic silicon compound or an organic silicon oxide is desirable, for example, can mention polysilane, polysilene, the organic SOG film, etc. although especially the molecular weight of these compounds is not limited -- desirable -- 200-100,100 -- 500-300,000 are more preferably good.

[0030] As an example, the following chemical formula 1-1 to 1-19, the compound shown in 2-1 to 2-13 can be mentioned. In addition, n in these chemical formulas and m express a positive integer.

[Formula 1]

1-1



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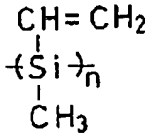

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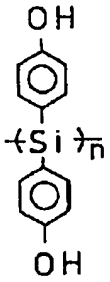

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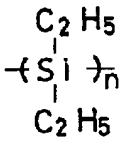

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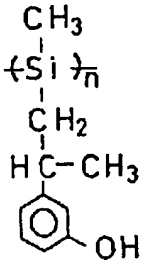

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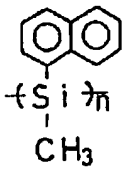

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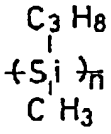

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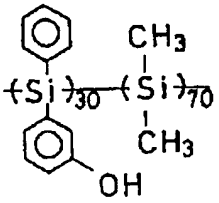

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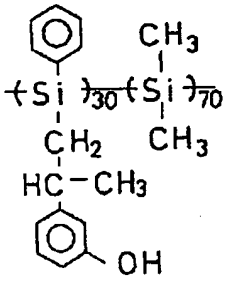
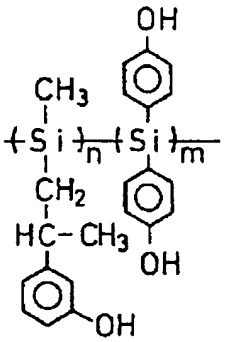
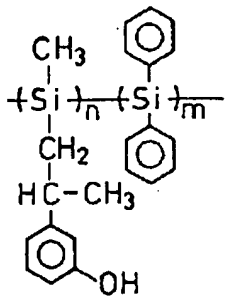
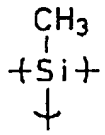


[Formula 2]

1-10 1-11 1-12

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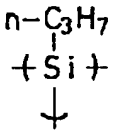
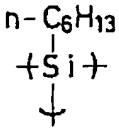
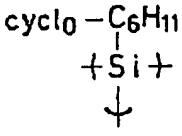
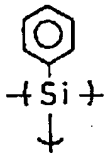
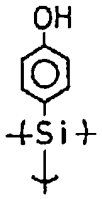
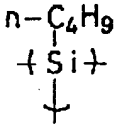
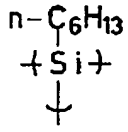
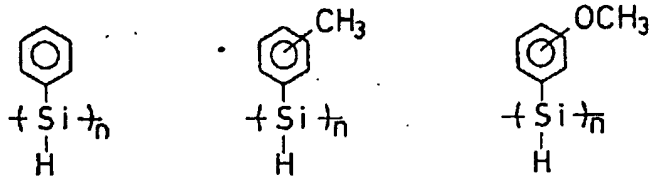




1-16 1-17 1-18 1-19

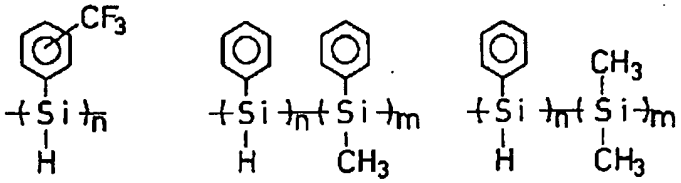





[Formula 3]

2-1 2-2 2-3



2-4 2-5 2-6



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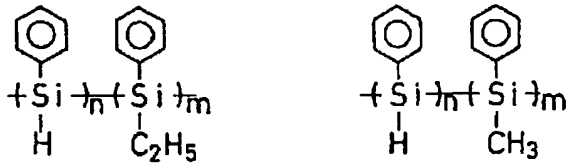

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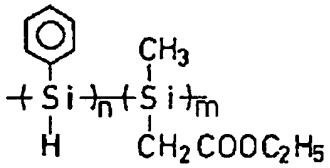

[Formula 4]

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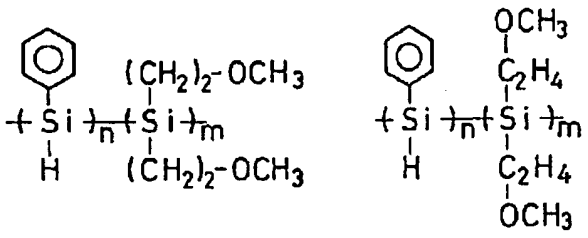
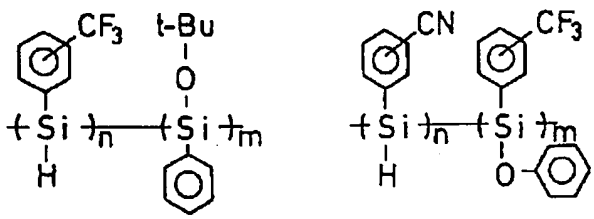


2-12 2-13



Desirably, said silicon compound and if needed, said liquefied constituent dissolves an additive in a solvent, and is obtained. Spreading afterbaking of this liquefied constituent is carried out on the processed layer which has the level difference section, and a flattening layer is formed by volatilizing and drying a solvent. In order to plan storage stability

if needed as an additive added by said liquefied constituent, the adhesion improver for raising adhesion with a thermal polymerization inhibitor and a base etc. is mentioned.
[0031] (The 2nd process) The 2nd process is a process which carries out pattern NINGU of said flattening layer so that it may become a mask layer at the time of said flattening layer performing processing of level difference circles, or an etching stopper layer.
[0032] Pattern NINGU of said flattening layer can form a resist layer for example, on a flattening layer, can form a resist pattern using photolithography, and can perform it by etching said flattening layer by using said resist pattern as a mask.
[0033] Etching of said flattening layer can use etching systems, such as a reactant plasma-etching method, a magnetron reactivity plasma-etching method, an electron beam plasma-etching method, a TCP etching method, an ICP etching method, or an ECR plasma-etching method.
[0034] Furthermore, it is desirable to perform the process which denaturalizes said flattening layer by which pattern NINGU was carried out. When said especially flattening layer is a silicon compound layer, it is desirable to perform at least one denaturation of oxidation, nitrogen-izing, and carbonization. When said denaturation is oxidation, said silicon compound layer is oxidized and it becomes a silicon oxide layer. When said denaturation is nitriding, said silicon compound layer is nitrided and it becomes a silicon nitride layer. When said denaturation is carbonization, said silicon compound layer is carbonized and it becomes a silicon carbide layer. In case any layer is used as a mask layer or an etching stopper layer, high dry etching resistance is shown.
[0035] When said denaturation is oxidization, it is desirable to carry out by supplying the ion or radical of oxygen to said silicon compound layer. It can carry out to oxidization of a silicon compound layer, exfoliation of the resist pattern at the time of pattern NINGU, and coincidence by using this approach. That is, association of silicon and silicon can be oxidized by irradiating a high energy beam under the ambient atmosphere to which oxygen exists in the layered product of a resist pattern and a silicon compound layer, carrying out ashing of the resist pattern. As a high energy beam, ultraviolet radiation, an electron beam, an ion beam, and an X-ray can be mentioned.
(The 3rd process) The 3rd process includes the process which etches the level difference section of a processed layer in the level difference section upper part of a processed layer by using as an etching stopper layer or a mask layer said flattening layer by which pattern NINGU was carried out. Said etching forms membranes in the level difference section of said processed layer, and may be performed to the matter formed of the membrane formation.
[0036]
[Example] Drawing 1 and drawing 2 show the sectional view showing one process of a trench capacitor formation process of having used this invention.
[0037] first, the SiO two-layer which acts as a mask of trench formation on a silicon substrate 11 beforehand as shown in drawing 1 (1) -- 17 was formed and pattern NINGU was carried out by the photolithography using a resist layer (not shown).
[0038] next, it is shown in drawing 1 (2) -- as -- SiO two-layer -- it etched by having used 17 as the mask, and the deep trench 12 was formed.
[0039] As shown in drawing 1 (3) through further two or more processes, the SiN layer 13 was formed in the wall of a trench (it is the same as that of drawing 3) 12, and the structure where it filled up with N+ polish recon layer 14 in the SiN layer 13 further was formed.
[0040] Next, the processing process including etching was given in the trench 12 of the processed layer in which the level difference section 12, i.e., a trench, was formed beforehand as mentioned above. Said processing process performed the 1st - the 3rd process which are shown below.
(The 1st process) the liquefied constituent which dissolved in the solvent the silicon compound which becomes the silicon substrate 11 (processed layer) in which said trench 12 was formed from a poly diphenyl silane first as the 1st process is shown in drawing 1 (4) -- spin coating -- carrying out - it dried and the flat silicon compound layer 16 was formed.
(The 2nd process) As shown in drawing 1 (5), the 2nd process formed the resist layer on the silicon compound layer 16, formed the resist pattern 18 using photolithography, and as shown in drawing 1 (6) below, it etched the silicon compound layer 16 by the RIE method by using a resist pattern 18 as a mask.
[0041] Etching conditions can take the selection ratio of the poly diphenyl silane 16 and a resist 18 50 to 100 or more by applying the gas which mixed Cl2:CF4:O2 gas by the ratio of 1:0.2:10.

[0042] Next, the denaturation process of said silicon compound layer 16 by which pattern NINGU was carried out was performed. The process made into the silicon oxide layer 19 as oxidizes and shows the silicon compound layer 16 by which pattern NINGU was specifically carried out to drawing 1 (7) was performed. At this process, it carried out by oxidizing association of silicon and silicon by irradiating O2 ion and a radical under the ambient atmosphere to which oxygen exists in the layered product of a resist pattern 18 and the silicon compound layer 16, carrying out ashing of the resist pattern.
[0043] Next, as shown in drawing 1 (8), i-polish recon layer 15 was formed in the trench 12.
[0044] Next, as shown in drawing 2 (9), chemical mechanical polish processing of the i-polish recon layer 15 front face was carried out, the silicon oxide layer 19 was exposed and flattening was carried out.
[0045] Next, as shown in drawing 2 (10), the silicon oxide layer 19 was used as the mask, and desired trench (it is the same as that of drawing 4) structure was acquired for etching of i-polish recon layer 5 by the RIE method. It is possible to take the selection ratio of the silicon oxide layer 19 and i-polish recon layer 15 50 or more because etching conditions use the conditions of HBr:O 2= 10:1.
[0046] Finally the silicon oxide layer 19 exfoliated at the back process.
[0047] As stated above, after forming a trench 12 in this example, the mask layer for processing in a trench 12 is formed. Therefore, ingredients other than a SiN layer with high processing of an aspect ratio difficult as said mask layer can also be used. moreover, the thing for which the silicon oxide layer obtained from the silicon compound layer which carried out spreading desiccation and obtained the liquefied constituent containing polysilane as said mask layer is used -- process tolerance -- it can be high, and the mask layer excellent also in etching resistance can be formed, and it can respond also to detailed-ization of a semiconductor device.
[0048]
[Effect of the Invention] Since the ingredient of said mask layer or an etching stopper layer and the width of face of selection of thickness can be expand since formation of the mask layer use in case processing of the process film which have the level difference section of said level difference circles be perform according to this invention, or an etching stopper layer be perform after level difference section formation as state above, and high processing of precision can be perform, it become possible to correspond to detailed-ization of a semiconductor device.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] Cross-section this schematic drawing which is applied to one example of this invention and in which showing the example of a process of the production process of a trench capacitor.
[Drawing 2] Cross-section this schematic drawing which is applied to one example of this invention and in which showing the example of a process of the production process of a trench capacitor.
[Drawing 3] Cross-section this schematic drawing showing one process of the production process of a trench capacitor.
[Drawing 4] Cross-section this schematic drawing showing one process of the production process of a trench capacitor.
[Drawing 5] Cross-section this schematic drawing showing the example of a process of the production process of the conventional trench capacitor.
[Description of Notations]
1 11 -- Silicon substrate
2 12 -- Trench
3 13 -- SiN layer
4 14 -- N+ polish recon layer
5 15 -- i-polish recon layer
6 -- SiN layer
7 17 -- SiO two-layer
18 -- Resist pattern
16 -- Silicon compound layer
19 -- Silicon oxide layer

[Translation done.]